

Tutorial On LVDS Channel Link

What is LVDS?

LVDS is a Low Voltage Differential Signaling device which extends the performance of the commonly used RS-422 differential data bus. RS-422 limits the frequency to the 20 MHz range. However, LVDS clock support is over 65MHz (66 MHz NSC 65 MHz TI) and improves the signal transmission cable length 30 to 100 feet. It also reduces EMI significantly.

Quick comparison

	RS-422	PECL	LVDS (RS-644)
Differential output voltage	± 2 - 5	± 600 - 1000 mV	± 250 - 450 mV
Receiver input threshold	± 200 mV	± 200 - 300 mV	± 100 mV
Data rate	< 30 Mbps	> 400 Mbps	> 400 Mbps

Standard cell comparison (Based in DS90C031/32)

	60 mA	32 - 6 mA	30 mA
Supply current (quad driver)	60 mA	32 - 6 mA	30 mA
Supply current (quad receiver)	23 mA	40 mA	10 mA

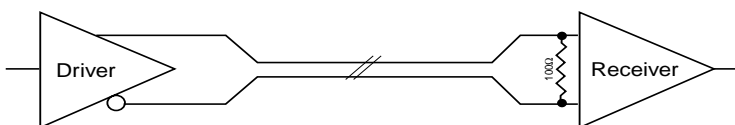
PULNiX started integrating LVDS into our cameras in 1995 when the TM-1040 with a 40 MHz clock was developed. The LVDS device is now called RS-644 and is pin-to-pin compatible with standard RS-422 transmitters and receivers. The typical transmitter and receiver is DS90C031 and DS90C032. These are equivalent to the 26LS032 and 26LS032 series of RS-422 device. If a frame grabber comes with an RS-644 input, it can take both RS-644 data and RS-422 data with extended cable length. Today, many frame grabbers support RS-644 differential parallel inputs up to the 40 MHz clock range.

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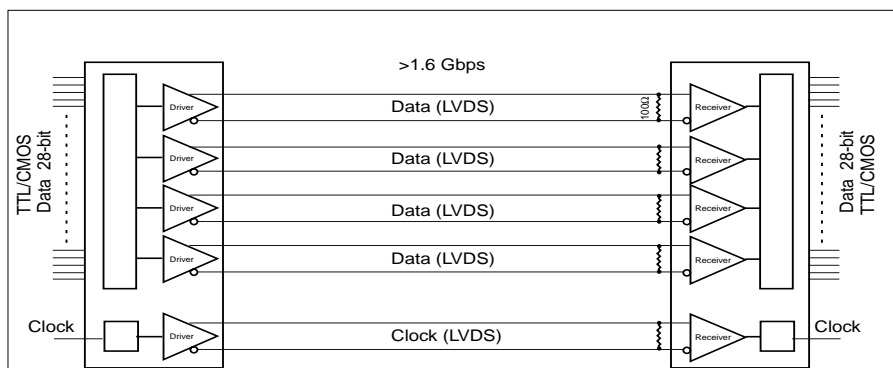
Channel Link™ is a trade name of National Semiconductor, the TI series is Flatlink™, and Silicon Image has Panel Link™. These are all compatible devices and designed to use LVDS technology with serializing parallel data in order to reduce cable numbers (similar technology as Hotlink). The total data rate goes up to 1.8 Gbps. The original development was done for digital communication applications. Now, the derivative devices are used in a digital flat panel (R, G, B) display bus. The Channel Link chip is a single chip architecture to handle 28-bit data and serialize the data into 5 twisted-pair cables. The receiver is also a single chip and decodes the serialized signal back to TTL 28-bit parallel data.

Which PULNiX cameras use LVDS output?

TM-1040 (40 MHz clock) and TM-6710 (25 MHz 8-bit x 2 or 50 MHz single 8-bit channel), TM-2000/2001 (37 MHz), PL5000 line scan (40 MHz data) and TMC-1000/6700, color camera (LVDS channel link).



Standard RS-422/RS-644 driver and receiver



Channel Link architecture:
The clock goes directly via one channel of the LVDS cable. The data bits are separated into 7-bit group and serialized. Each serialized 7-bit data uses one channel. Total 4 channels are used for 28-bit data (24-bit RGB and sync signals) plus one channel of clock.

Comparing the advantages of channel link.

1. Cable cost and size

Normal RS-422 or RS-644 digital color output is a parallel output in a 24-bit (RGB x 8-bit) data format and it requires minimum 28 pairs of cable including clock, H sync, V sync and Control Signal and Ground. This means minimum 56 conductors in a well shielded jacket. It is heavy and rigid and expensive. The assembly of the cable to connectors such as 6-pin, 100-pin SCSI-2 connector or any miniature connector is very difficult (labor and cost is high). The PULNiX TMC-1000 series digital output cable uses only 8-pair double-shielded cable with 15-pin connector.

2. Space and power saving

Typical RS-422 driver or receiver is a quad package (4 devices) and needs 7 ICs (16-SOIC) to drive or receive 28-bit data, whereas the channel link uses a single chip (56-TSSOP) almost the same size as a 16-SOIC package. It also reduces the power consumption due to CMOS design and the low power nature of LVDS.

Why is PULNiX the first camera manufacturer to use the Channel Link?

PULNiX has always been a leading company in new technology. When the TMC-1040 was developed, PULNiX sent the LVDS chip to frame grabber manufacturers to interface the camera. Today RS-644 is an industrial standard for camera and frame grabber manufacturers. The Channel Link will be the same situation. Already a number of frame grabber companies have stated designing in the channel link. This is not only for color cameras, but can be used for multi-tap digital data bus (16, 24, 32-bit, etc.) applications in black and white, line scan and general digital cameras for high frame rate communication. The interface and the protocol is not unique to PULNiX. The pin configuration for connectors or cables is the standard in 24-bit color flat panel display standard. The following channel assignment is the FPD (Flat Panel Display) standard.

Device pin No.		Signal	Channel No.	PULNiX Cable (15CL-02) & Connector pins
Transmitter clock in	Receiver clock out	Clock (Dot clock)	Clock CH ---	01CH: clk+ (pin 1), clk- (pin 9)
0	0	Red 0 (MSB)	CH 1 -----	02CH: 0+ (pin 2), 0- (pin 10)
1	1	Red 1		
2	2	Red 2		
3	3	Red 3		
4	4	Red 4		
5	5	Red 7 (LSB)	CH 4	
6	6	Red 5	CH 1	
7	7	Green 0	CH 1	
8	8	Green 1	CH 2 -----	03CH: 1+ (pin 3), 1- (pin 11)
9	9	Green 2	"	
10	10	Green 6	CH 4 -----	05CH: 3+ (pin 5), 3- (pin 13)
11	11	Green 7	"	
12	12	Green 3	CH 2	
13	13	Green 4		
14	14	Green 5		
15	15	Blue 0		
16	16	Blue 6	CH 4	
17	17	Blue 7	"	
18	18	Blue 1	CH 2	
19	19	Blue 2	CH 3 -----	04CH: 2+ (pin 4), 2- (pin 12)
20	20	Blue 3		
21	21	Blue 4		
22	22	Blue 5		
23	23	Res	CH 4	
24	24	H sync	CH 3	
25	25	V sync	"	
26	26	DEN	"	
27	27	Red 6	CH 4	

Other pins for PULNiX cable
 06, Vinit+ (pin 6), Vinit- (pin 14)
 07, Integ+ (pin 7), Integ- (pin 15)
 08, GND (pin 8)